

Abstract of the Disclosure

Structures are provided which improve performance in integrated circuits. The structures include a diffusion barrier and a seed layer in an integrated circuit both formed using a low energy ion implantation followed by a selective deposition of metal lines for the integrated circuit. The low energy ion implantation allows for the distinct placement of both the diffusion barrier and the seed layer. Structures are formed with a barrier/adhesion layer deposited in the number of trenches using a low energy ion implantation, e.g. a 100 to 800 electron volt (eV) ion implantation. A seed layer is deposited on the barrier/adhesion layer in the number of trenches also using the low energy ion implantation. Such structures include aluminum, copper, gold, and silver metal interconnects.

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